Amendments to the Claims

1. (*Currently Amended*) A method of manufacturing on a substrate ~~(50)~~ a 2-transistor memory cell ~~(10)~~ comprising a storage transistor having a memory gate stack ~~(1)~~ and a selecting transistor, there being a tunnel dielectric layer between the substrate ~~(50)~~ and the memory gate stack ~~(1)~~, the method comprising:

forming the memory gate stack ~~(1)~~ by providing a first conductive layer ~~(52)~~ and a second conductive layer ~~(54)~~ and etching the second conductive layer ~~(54)~~ thus forming a control gate and etching the first conductive layer ~~(52)~~ thus forming a floating gate,

the method furthermore comprising, before etching the first conductive layer ~~(52)~~, forming spacers ~~(81)~~ against the control gate in the direction of a channel to be formed under the tunnel dielectric layer ~~(51)~~, and thereafter using the spacers ~~(81)~~ as a hard mask to etch the first conductive layer ~~(52)~~ thus forming the floating gate.

2. (*Currently Amended*) A method according to claim 1, wherein the spacers ~~(81)~~ are formed from a dielectric material ~~which has~~ having an oxygen diffusion through the material ~~which is~~ that is an order of magnitude smaller than oxygen diffusion through oxide spacers.

3. (*Original*) A method according to claim 2, wherein the dielectric material ~~which has~~ having an oxygen diffusion through the material ~~which is~~ that is an order of magnitude smaller than oxygen diffusion through oxide spacers ~~is one~~ includes one or more of silicon nitride, silicon carbide or metal oxide.

4. (*Currently Amended*) ~~A method according to any of the previous claims,~~ A method according to claim 1, furthermore comprising,

_____before forming the memory gate stack ~~(1)~~, applying the tunnel dielectric layer ~~(51)~~ on the substrate, and

_____after formation of the memory gate stack ~~(1)~~, removing the tunnel dielectric layer ~~(51)~~ by a selective etching technique at least at a location where the selecting transistor is to be formed, the selective etching technique preferentially etching the tunnel dielectric layer ~~(51)~~ compared to the substrate ~~(50)~~.

5. (*Currently Amended*) ~~A method according to any of the previous claims,~~ A method according to claim 1, comprising,

_____after etching of the first conductive layer ~~(52)~~, providing a floating gate dielectric ~~(102)~~ next to the formed floating gate and at the same time providing an access gate dielectric ~~(101)~~.

6. (*Currently Amended*) ~~A method according to any of the previous claims,~~ A method according to claim 1, the memory gate stack ~~(1)~~ comprising an interlayer dielectric layer ~~(53)~~ between the first conductive layer ~~(52)~~ and the second conductive layer ~~(54)~~, the method furthermore comprising

_____removing part of the interlayer dielectric layer ~~(53)~~ after forming the control gate but before forming the spacers ~~(81)~~.

7. (*Currently Amended*) ~~A method according to any of the previous claims,~~ A method according to claim 1, the selecting transistor comprising an access gate ~~(103)~~, the method comprising

_____forming the access gate ~~(103)~~ while the spacer ~~(81)~~ at the access gate side is still present.

8. (*Currently Amended*) A 2-transistor memory cell ~~(10) comprising~~ comprising,

a storage transistor ~~(1)~~ and

a selecting transistor, the storage transistor comprising a floating gate ~~(52)~~ and a control gate ~~(54)~~, wherein the control gate ~~(54)~~ is smaller than the floating gate ~~(52)~~, and spacers ~~(81)~~ are present next to the control gate ~~(54)~~.

9. (*Currently Amended*) A memory cell ~~(10)~~ according to claim 8, wherein the spacers ~~(81)~~ are made from a dielectric material ~~which has~~ having an oxygen diffusion through the material ~~which is~~ that is an order of magnitude smaller than oxygen diffusion through oxide spacers.

10. (*Currently Amended*) ~~A memory cell (10) according to claim 8 or 9,~~ A memory cell according to claim 8, the selecting transistor comprising an access gate ~~(103)~~, a

spacer ~~(81)~~ being present between the control gate ~~(54)~~ and the access gate ~~(103)~~ and a floating gate dielectric ~~(102)~~ being present between the floating gate ~~(52)~~ and the access gate ~~(103)~~, wherein the spacer ~~(81)~~ is thicker than the floating gate dielectric ~~(102)~~.

11. (*Currently Amended*) ~~An electronic device comprising a memory cell (10) according to any of claims 8 to 10.~~
An electronic device comprising a 2-transistor memory cell, the 2-transistor memory cell including,

a storage transistor and

a selecting transistor, the storage transistor comprising a floating gate and a control gate, wherein the control gate is smaller than the floating gate, and spacers are present next to the control gate.

12. (*New*) The electronic device as recited in claim 11, wherein the spacers are made from a dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than the oxygen diffusion through the oxide spacers.

13. (*New*) The electronic device as recited in claim 12, wherein the selecting transistor includes,

an access gate,

a spacer being present between the control gate, and

the access gate and a floating gate dielectric being present between the floating gate and the access gate, wherein the spacer is thicker than the floating gate dielectric.